Remarks

Claims 4, 5, and 12 are presently pending and stand rejected. Claims 1-3 and 6-11 are cancelled without prejudice.

Claim 4 was also rejected under 35 U.S.C. § 102(f) on the grounds that "applicant did not invent the claimed subject matter". Examiner has argued that "The above recited limitations, such as 'first circuitry' and 'second circuitry' are inherent to the convention hardware emulator because it is a device with a large amount of logic and other circuitry with highly configurable connections, further a script checks the capacity of the hardware emulator to determine whether the hardware emulator has sufficient logic and circuitry to realize the design".

Assignee respectfully traverses the rejection. First, Specification 0006 does not teach "a second circuitry configured to realize and verify the second system on another chip *while the first circuit verifies the first system on chip*, the second circuitry directly connected to the first circuitry". Secondly, it is noted that the claim limitation is in the past tense, "configured" as opposed to "configurable". Therefore, even if the emulator has the capacity, mere capacity is not configured.

Claim 4 was also rejected under 35 U.S.C. § 102(e) as being anticipated by Rohlfleisch. Examiner has made citation to Rohlfleisch [0039]. However, Rohlfeisch [0039] states that "Advantageously, the emulator circuits 104, 108 and the emulator interface circuit 110 permit an SOC designer or programmer to test, evaluate, and/or debug the processor core 102 and/or the other core 106 using the emulation interface circuit 110." Note, however that "emulator circuits 104, 108" are in fact, <u>two</u> emulator circuits. In contrast, Assignee claims "<u>a</u> hardware emulator for verifying a first system on a chip and a second system on another chip" – noting the use of the singular context in the claim.

Additionally, Rohlfleisch also does not teach "a hardware emulator for verifying a first system on a chip and a second system on another chip, said hardware emulator comprising: a first circuitry configured to realize and verify the first system on a chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry; and a second circuitry

configured to realize and verify the second system on another chip while the first circuit verifies the first system on chip, the second circuitry *directly* connected to the first circuitry." As noted above, "the emulator circuits 104, 108 and the emulator interface circuit 110 permit an SOC designer or programmer to test, evaluate, and/or debug the processor core 102 and/or the other core 106". Clearly, emulator circuit 104 and emulator circuit 108 are not *directly* connected to each other.

For convenience, Rohlfleisch, Figure 1 is shown below.

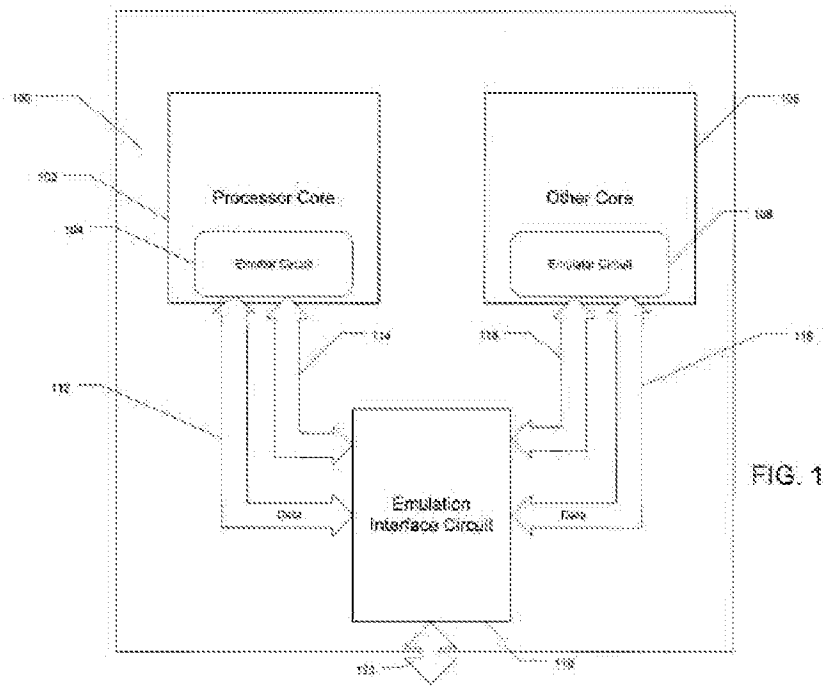

FIG. 1

Rohlfleisch, Figure 1.

Assignee respectfully submits that the foregoing is not "just a general allegation that claims to define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes…". Assignee points to the claim language, "the second circuitry *directly* connected to the first circuitry", and how it distinguishes over Rohlfleisch – clearly the 104 and 106 are not directly connected. Assignee submits that connection of 104 and 106 to the emulation interface circuit is not "directly" connected.

Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claims 4, 5, and 12.

Conclusion

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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